145 Adams Avenue, Hauppauge, NY 11788, USA
Tel: 1.631.435.1110 Fax: 1.631.435.1824
www.centralsemi.com

Package Qualification Summary

Package: BR DFN-A

Scope

This document summarizes the Case Type Qualification and reliability tests applied to the Central Semiconductor package specified. The tests performed are capable of inducing semiconductor device and packaging related failures. The objective of these harsh tests is to determine whether failures occur in an accelerated manner compared to normal use conditions for a representative sample size. Passing all appropriate reliability tests (no failures) for a representative sample size Qualifies the package. This Qualification summary is a generic qualification for a range of use conditions and is not applicable at extreme use conditions, for example military applications, automotive under-the-hood applications, uncontrolled avionics environments, or 2nd level reliability considerations.

Qualification Test Descriptions

The description of Qualification Tests listed below are provided as a summary. Refer to the applicable specification indicated in parenthesis for additional details.

External Visual Inspection (JESD22-B101)
An examination of the external surfaces, construction, marking, and workmanship of a finished package or component. External visual is a noninvasive and nondestructive test.

Physical Dimensions (JESD22-B100)
The purpose of this test is to determine whether the external physical dimensions of the device, in all package configurations, are in accordance with the applicable procurement document. The physical dimensions test is nondestructive.

Marking Permanency (JESD22-B107) – Only applicable for devices marked with ink
The mark permanency test subjects package marking to solvents and cleaning solution commonly used for removing solder flux on circuit boards to ensure the marking will not become illegible. Devices and a brush are immersed into one of three specified solvents for one minute, and then removed. The devices are then brushed ten strokes. After they are rinsed and dried, the devices are examined for legibility according to specified criteria.

Lead Integrity (JESD22-B105)
The lead integrity test provides tests for determining the integrity of devices leads, welds and seals. Devices are subjected to various stresses including tension, bending fatigue and torque appropriate to the type of lead. Devices are then examined under optical microscope to determine any evidence of breakage, loosening or motion between the terminal and device body.

Co-planarity (JESD22-B108)
The purpose of this test is to measure the deviation of the terminals (leads or solder balls) from co-planarity at room temperature for surface-mount semiconductor devices.

Internal Visual Inspection (MIL-STD-750 method 2075)
The purpose of this examination is to verify that internal materials, design and construction are in accordance with the applicable acquisition document. The device shall be examined under a sufficient magnification to verify the requirements as per applicable design documentation.

Bond Strength - Wire Pull (MIL-STD-750 method 2037 test condition C/D)
The purpose of this test method is to measure bond strengths, evaluate bond strength distributions, or determine compliance with specified bond strength requirements of the applicable acquisition document. This test may be applied

to the wire-to-die bond, wire-to-substrate bond, or the wire-to-package lead bond inside the package of wire-connected microelectronic devices bonded by soldering, thermocompression, ultrasonic, or related techniques.

Die Shear (MIL-STD-750 method 2017 test condition A)
The purpose of this test method is to establish the integrity of the semiconductor die attachment to the package header or other substrate.

Die Attach Method Verification (MIL-STD-750 method 2017)
The purpose of this test method is to confirm the proper die attach method is used in accordance with the applicable acquisition document. Decapsulated devices are visually examined under optical microscope to verify the die attach method.

Charged Device Model (CDM) (JS-002-2018)
This test is used to simulate situations that happen in manufacturing environments such as mechanical device handling where devices slide down shipping tubes or test handlers that build up a charge that's subsequently discharged to ground.

Human Body Model (HBM) (JS-001-2017)
This test is used to simulate situations that replicate HBM type failures.

Electrical Parameters Assessment (DC Electrical) (JESD86)
This standard describes methods for obtaining electrical data with the intent is to assess the device's response function for specific parameters over time and under defined application environment (operating temperature, voltage, humidity, input/output levels, noise, power supply stability etc.) pre or post reliability stress test.

Gate Charge Test (JESD24-2):
Measures the input charge of insulated gate-controlled power devices such as power MOSFETs and IGBTs.

Capacitance Test (MIL-STD-750 Method 4001)
Measures the capacitance across the device terminals under specified DC bias and AC signal voltages.

Switching Time Test (MIL-STD-750 Method 3472)
Measures the pulse response (td(on), tr, td(off), tf) of power MOSFET or transistor devices under specified conditions.

Surge Current Test (MIL-STD-750 Method 4066)
Subjects the device (diodes) under test (DUT) to high current stress conditions to determine the ability of the device chip and contacts to withstand current surges. This is intended to verify a non-repetitive surge rating where there is sufficient time between surges to permit the device temperature to return to its original value. Surge current is applied in the forward direction to signal diodes and rectifier diodes, and in the reverse direction to voltage regulator (Zener) diodes.

Thermal Resistance Test (MIL-STD-750 method 3151)
The purpose of this test is to measure the temperature rise per unit power dissipation of the designated junction above the case of the device or ambient temperature, under conditions of steady state operation.

Reverse Recovery Time (Trr) Measurement (MIL-STD-750 method 4031)
The purpose of this test is to measure the reverse recovery time of signal, switching, and rectifier diodes by observing the reverse transient current versus time when switching from a specified forward current to a reverse biased state in a specified manner.

Resistance to Solder Shock (JESD22-B106)
This test method is used to determine whether solid state devices can withstand the effect of the temperature shock to which they will be subjected during soldering of leads in a solderwave process and/or solder fountain (rework/replacement) process.

Solderability (MIL-STD-750 method 2026)
The solderability test is used to determine the ability of package leads wetted by solder. This test verifies that the method of lead treatment to facilitate solderability is satisfactory and will allow successful solder connection to designated surface.

High Temperature Storage Life/Bake Test (JESD22-A103)
The high temperature storage test is typically used to determine the effects of time and temperature, under storage conditions, for thermally activated failure mechanisms and time-to failure distributions of solid state electronic devices. During the test, accelerated stress temperatures are used without electrical conditions applied.

High Temperature Reverse Bias (HTRB) (JESD22-A108)
The HTRB test is configured to reverse bias major power handling junctions of the device samples. The devices are characteristically operated in a static operating mode at, or near, maximum-rated breakdown voltage and/or current levels.

High Temperature Gate Bias (HTGB) (JESD22-A108)
The HTGB test biases gate or other oxides of the device samples. The devices are normally operated in a static mode at, or near, maximum-rated oxide breakdown voltage levels.

Preconditioning of Non-hermetic Surface Mount Devices (JESD22-A113)
The typical use of surface mount devices (SMD) involves subjecting the devices to elevated temperatures, which combined with moisture in the package can induce internal package damage that could be a qualification concern. Preconditioning of SMD packages is used to simulate the effects of board assembly on moisturized packages, prior to testing. During preconditioning, test samples are subjected to temperature cycling (optional), dry bake, moisture soaking, solder reflow simulation, flux, rinse, dry, an electrical test before reliability testing.

Accelerated Moisture Resistance – Unbiased Autoclave (JESD22-A102)
This test method applies primarily to moisture resistance evaluations and robustness testing to identify failure mechanisms internal to the package and is destructive. Samples are subjected to a condensing, highly humid atmosphere under pressure to force moisture into the package under accelerated conditions to uncover weaknesses such as delamination and metallization corrosion.

Temperature Cycling Test (JESD22-A104, MIL-STD-750 method 1051)
Temperature cycling test accelerates the effects that changes in the temperature will cause damage between different components within the specific die and packaging system due to different thermal expansion coefficients. During testing devices are inserted into a chamber where the interior is cycled between specified temperatures and held at each temperature for a minimum of ten minutes. Temperature extremes depend on the condition selected in the test method.

Thermal Shock (JESD22-A106)
This test is conducted to determine the resistance of a part to sudden exposure to extreme changes in temperature and to the effect of alternate exposures to these extremes.

Steady-State Temperature-Humidity Bias (THB) (JESD22-A101)
The Steady-State Temperature-Humidity Bias test is performed to evaluate the reliability of non-hermetic packaged devices in humid environments. Temperature, humidity, and bias conditions are applied to accelerate the penetration of moisture through the external protective material (encapsulant or seal) or along the interface between the external protective material and the metallic conductors which pass through it.

Highly Accelerated Temperature and Humidity Stress Test (HAST) (JESD22-A110)
The Highly-Accelerated Temperature and Humidity Stress Test is performed for the purpose of evaluating the reliability of non-hermetic packaged solid-state devices in humid environments. It employs severe conditions of temperature, humidity, and bias which accelerate the penetration of moisture through the external protective material (encapsulant or seal) or along the interface between the external protective material and the metallic conductors which pass through it. The stress usually activates the same failure mechanisms as the Steady-State Temperature-Humidity Bias test (JESD22-A101).

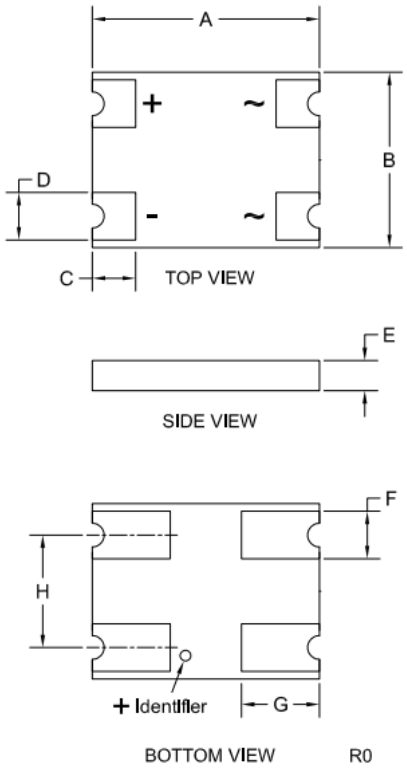
Helium Fine Leak Test (MIL-STD-883 method 1014 condition A1)
The purpose of this test is to determine the hermeticity of semiconductor devices with designed internal cavities such as ceramic and metal packages for leak rates generally below 10^{-5} atm-cc/s. The test is done for DUTs by keeping them in a chamber with appropriate pressure and duration of He gas. The leak rate detection is performed with a vacuum chamber and a mass spectrometer-type leak detector.

Gross Leak Test (MIL-STD-750 method 1071 test condition C)
The purpose of this test is to determine the hermeticity of semiconductor devices with designed internal cavities such as ceramic and metal packages for leak rates above 10^{-5} atm-cc/s . DUTs are kept in a chamber with appropriate perfluorocarbon liquid, pressure, and duration. They are then immersed in a perfluorocarbon liquid of higher boiling point set at +125°C ±5°C and observations are made to detect gas (vapor) leakage.

Mechanical Shock (JESD22-B110)
The Mechanical Shock Test is intended to evaluate component(s) for use in electrical equipment. It is intended to determine the compatibility of the component(s) to withstand moderately severe shocks as a result of suddenly applied forces or abrupt change in motion produced by handling, transportation or field operation.

Package Details
BR DFN-A Case

Mechanical Drawing



DIMENSIONS				
	INCHES		MILLIMETERS	
SYMBOL	MIN	MAX	MIN	MAX
A	0.409	0.417	10.40	10.60
B	0.315	0.323	8.00	8.20
C	0.073	0.085	1.85	2.15
D	0.083	0.091	2.10	2.30
E	0.049	0.061	1.25	1.55
F	0.083	0.091	2.10	2.30
G	0.138	0.146	3.50	3.70
H	0.201	0.209	5.10	5.30

BR DFN-A (REV: R0)

Part Marking: 5-6 Character Alpha/Numeric Code

Qualification Summary

P/N: CBRDFA4-100

Test	Qty	Reference	Conditions	Pass/Fail
ESD HBM	3	JS-001-2017	Start at 2000 V. Step down voltage by 1/2 if failure is observed. 3 devices must pass at a given ESD voltage level. Apply voltage pulse across each permutation of pins on DUT.	Pass
Pre-Cond	500	JESD22-A113	Sequence: initial electrical test, visual inspection, temperature cycle, bake, moisture soak, reflow, flux soak, clean & dry, and final electrical test.	Pass
Solder Shock	5	JESD22-A111 and JESD22-B106	Pb free: T =270°C ±5°C, Dwell=7s +2/-0 Sn/Pb: T =260°C ±5°C, Dwell=10s +2/-0 Thru-hole devices submerge to case, SMDs fully submerge	Pass
Solderability	15	MIL-STD-750 TM2026	Steam Age: T=93°C +3/-5°C. Non Pb-free Dip: T=215°C +/-5°C, Pb-free Dip: T=245°C +/-5°C, Dwell time = 5+/-0.5sec	Pass
Bake	77	JESD22-A103	150°C (-0/+10)°C or specified temperature. 1000 hours	Pass
HTRB	77	JESD22-A108	T=125°C, t = 1000 hours Bias conditions per device datasheet.	Pass
UHAST	77	JESD22-A110	T = 130°C, RH = 85%, t = 96 hrs or T = 110°C, RH = 85%, t = 264 hrs	Pass
Temp Cycle	77	JESD22-A104 & MIL-STD-750 TM1051.	1000 cycles. Dwell time = 15 min Ta = -65°C to +150°C	Pass
Thermal Shock	77	JESD22-A106	100 cycles, dwell time = 5 min, -65°C to +150°C, max transfer time = 20 sec.	Pass
THB	77	JESD22-A101	T = 85°C, RH = 85%, t = 1000 hrs Bias conditions per device datasheet.	Pass